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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,889	02/28/2002	Michael J. Rendon	SC11814TP	4132

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MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
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EXAMINER
DIAZ, JOSE R

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,889	RENDON ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (US Pat. No. 6,057,212) in view of Talwar et al. (US Pat. No. 6,300,208 B1), cited by applicant.

Regarding claims 1-2, 13, 16, and 19, Chan et al. teach a method of forming a semiconductor device comprising the steps of: placing an energy absorbing layer (5, 320) above the substrate (1', 310) (see figs. 1 and 3); forming a semiconductor layer (3, 335) above the energy absorbing layer (see Fig. 3); forming a control electrode (301) (see fig. 3); forming first and second current electrodes (S,D) within the semiconductor

layer (see fig. 3). However, Chan et al. is silent with respect to the limitation of annealing or exposing the substrate to an energy source to electrically activate the source/drain regions. Talwar et al. teaches that is well known in the art to activate the source/drain regions (5,6) by laser annealing (10) the substrate (see fig. 2F and col. 7, lines 15-20) using a laser with a wavelength of 100-1200 nm (see col. 7, lines 18-21). Chan et al. and Talwar et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to laser anneal the substrate of Chan et al. using the laser method taught by Talwar et al. The motivation for doing so, as is taught by Talwar et al., is to activate the source/drain regions (col. 7, lines 13-15). Therefore, it would have been obvious to combine Chan et al. with Talwar et al. to obtain the invention of claims 1-21.

With regards to the limitation that the first and second current electrodes are activated by receiving heat from the energy absorbing layer, Talwar et al. discloses a laser annealing step in which the energy source is controlled by choosing an appropriate wavelength (e.g. 100-1200nm) (see col. 7, lines 18-21). As taught by applicant, the use of such a laser annealing method and wavelength will inherently heat the energy-absorbing layer of Chan et al. for activating the first and second current electrodes.

Regarding claim 3, Chan et al. teach that the semiconductor device is formed by bonding the semiconductor layer (3) to the energy-absorbing layer (5) (see Fig. 1).

Regarding claims 4-5, Talwar et al. teaches that is well known in the art to control the energy source by setting the wavelength of the light source to about 800 nm or more (see col. 7, lines 18-21).

Regarding claim 6, Talwar et al. teaches that is well known in the art to expose the energy-absorbing layer to an energy source (10) by positioning the energy source (10) to be above the integrated transistor device the substrate (2) (see fig. 2F).

Regarding claim 7, Chan et al. teach that the absorbing material (5, 320) is made of a refractory metal (see col. 4, line 8-10).

Regarding claim 8, Chan et al. teach that the semiconductor layer (3, 335) has at least one of Si, Ge or GaAs (see col. 4, lines 2-3, and col. 5, lines24-26).

Regarding claim 9, Chan et al. further teach providing an insulating layer (4, 325) between the energy absorbing layer and the control electrode (see Figs. 1 and 3).

Regarding claim 10, Chan et al. further teaches that the substrate is a SOI substrate (see col. 3, lines 66-67) or may include an insulating layer (315) above the substrate (310) (see fig. 3).

Regarding claims 11 and 20, Chan et al. further teaches providing an adhesion layer (325) between the energy-absorbing layer (4, 320) and the semiconductor layer (3, 335) (see Figs. 1 and 3).

Regarding claims 12, 14 and 18, Chan et al. further teaches the limitation of forming an isolation region (see the region that is at each side of the contact 345 and above the energy absorbing layer 320 in Fig. 3).

Regarding claim 15, Talwar et al. teaches that it is well known in the art to process a portion of the control electrode to comprise silicon having a higher melting temperature than the first and second current electrodes (see col. 5, lines 40-45) and processing the first and second current electrodes to comprise amorphous silicon (see col. 7, lines 7-12).

Regarding claim 17, Chan et al. further teaches a SOI device (see col. 2, lines 42-48).

Regarding claim 21, Chan et al. and Talwar et al. teach the claimed limitations as stated above in the rejections of claims 1, 13, 16, and 19. With regards to the claimed resistivity, Chan et al. and Talwar et al. teach a process of forming a device in which the source and drain regions are activated by a laser annealing step. Please note that it is inherent that during such activation or annealing step the resistivity of the source and drain a region is improved. Therefore, it would have been obvious to one of ordinary skill in the art to anneal the source and drain regions such that the resistivity is improved from 0.1 ohm-cm to 0.001 ohm-cm, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

➢ Applicant's arguments, see remarks on pages 2-3, filed July 16, 2003, with respect to the rejection(s)of claim(s) 1-21 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new ground(s) of rejection is made in view of Talwar et al. (US Pat. No. 6,300,208 B1). Talwar et al. discloses a well known process in which the source and drain regions are activated by a laser annealing step in which the wavelength of the light source is set to a range similar to applicant's invention.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD

GEORGE ECKERT
PRIMARY EXAMINER